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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,625	12/19/2005	Andrei Terechko	NL02 1505 US	8452

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
11/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,625	TERECHKO ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

2. In view of the appeal brief filed on 8/30/07, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Thomas Lee

/Thomas Lee/

3. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Claim Rejections - 35 U.S.C. § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In claim 18, such as the limitation "a hardware definition program defining the circuit arrangement of claim 1". The hardware definition program can not defining the hardware circuit arrangement of claim 1.

5. Claim 18 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 18 is not limited to tangible embodiments. In view of Applicant's disclosure, specification page 9, line 28-page 10, line 1, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments and intangible embodiments such as transmissions and communication links (digital/analog) which are non-statutory subject matter, such as the digital and analog communication links are not tangible media. As such, the claim is not limited to statutory subject matter and is therefore non-statutory. The signal bearing tangible medium as described in the specification and in the claim includes communication links; and a computer program on communication links is not a proper manufacture under 35 U.S.C. 101. For purposes of examination it will be interpreted that the medium is statutory subject.

Claim 18 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. If a computer program is not executed, then it is just a program pro se, therefore it does not fall within the statutory subject matter. As such patentability can not be accorded.

6. Claims 1-9 and 11-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Launiainen (Launiainen), U.S. patent no. 7,114,089.

As per claim 1, Launiainen discloses a circuit arrangement [fig. 3b], comprising a plurality of hardware resources [col. 5, lines 19-25], wherein each hardware resources has a power mode configurable between at least first and second power consumption states [col. 53, lines 30-41]; and a processor [1, fig. 5] coupled the plurality of hardware resources [figures 3a, 5], the processor configured to process program code that includes at least one power control instruction that includes an operand having power control information disposed therein, wherein the processor is configured to process the power control instruction by selectively setting power modes of at least two hardware resources among the plurality of hardware resources based upon the power control information disposed in the power control instruction, and wherein the processor is further configured to maintain the power modes of the power modes of the at least two hardware resources to that specified in the power control instruction while processing at least one subsequent instruction in the program code [figures 3b, 6; col. 6, lines 11-60; col. 7, lines 47-27].

As per claim 2, Launiainen discloses the power control instruction further includes an opcode that uniquely identifies the power control instruction [fig. 6; col. 6, lines 11-47; col. 8, lines 10-20].

As per claim 3, Launiainen discloses that a support register that stores power modes state information for the plurality of hardware resources [col. 5, lines 19-27]; and enable logic coupled to the support register and configured to control the power modes of the plurality of hardware resources responsive to the power modes state information stored in the support register, wherein the processor is configured to selectively set the power modes of the at least two hardware resources by storing the power control information from the power control instruction in the support register [col. 6, lines 11-60; col. 7, line 47-col. 8, line 27].

As per claim 4, Launiainen discloses that the support register comprises a power modes register [col. 6, lines 11-60; col. 7, lines 47-27].

As per claim 5, Launiainen discloses that the support register includes additional status information that is unrelated to power dissipation control [col. 6, lines 11-60; col. 7, line 47-col. 8, line 27].

As per claim 6, Launiainen discloses that a subset of the plurality of hardware resources comprises a plurality of banks of registers defining a register file, wherein the enable logic includes a plurality of enable circuits, each associated with a bank of register from the plurality of banks of registers, and each configured to selectively disable its associated bank of registers responsive to an enable signal wherein the enable logic is further configured to generated the enable signal for each bank of

registers from the power modes state information stored in the support register [fig. 3b; col. 5, lines 19-25; col. 6, lines 11-60; col. 7, line 47-col. 8, line 27].

As per claim 7, Launiainen discloses that each bank of registers includes at least one clock input, address input and data input, and wherein the enable circuit for each bank of registers is configured to selectively gate off the clock, address and data inputs for its associated bank of registers in response to the enable signal provided thereto [figure 4; col. 5, lines 11-27; col. 6, lines 11-50; col. 7, lines 47-64].

As per claim 8, Launiainen discloses that each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder [fig. 3b; col. 5, lines 11-27].

As per claim 9, Launiainen discloses that the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprise an operation among a plurality of operations in an explicitly parallel instruction [col. 6, lines 11-60; col. 7, lines 47-27].

As per claim 11, Launiainen discloses a superscalar processor [col. 1, lines 59-60].

As per claim 12, Launiainen discloses that the processor is configured to assign a side effect to the power control instruction to limit run-time speculation thereof [col. 6, lines 11-50; col. 7, lines 47-64].

As per claim 13, Launiainen discloses that the power control information in the operand identifies a register within which power modes state information for the at least

two hardware resources is stored, and wherein the processor is configured to selectively set the power modes of the at least two hardware resources by retrieving the power modes state information from the register identified by the power control information in the operand [col. 6, lines 11-60; col. 7, line 47-col. 8, line 27].

As per claim 14, Launiainen discloses that the pluralities of hardware resources are disposed in the processor [fig. 3b].

As per claim 15, Launiainen discloses that at least one hardware resource is disposed outside of the processor but on the same integrated circuit as the processor [fig. 3a].

As per claim 16, Launiainen discloses that at least one hardware resource is disposed on a separate integrated circuit from the processor [fig. 5].

As per claim 17, Launiainen discloses an integrated circuit [fig. 3a].

As per claim 18, Launiainen teaches the claimed system. Therefore, Launiainen teaches the claimed computer program storing in a medium to carry out the system.

As to claims 19-30, Claims 1-9 and 11-16 basically are the corresponding elements that are carried out the method of operating steps in claims 19-30. Accordingly, claims 19-30 are rejected for the same reason as set forth in claims 1-9 and 11-16.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Launiainen (Launiainen), U.S. patent no. 7,114,089 in view of what was well known in the art, as exemplified by Dinechin (Dinechin), U.S. publication no. 2003/0177482.

As per claim 10, Launiainen fails to disclose that a VLIW processor and an EPIC processor.

Examiner takes Official Notice that a VLIW processor and an EPIC processor are well known in the art, evidence of which may be found in

Dinechin: figure 1; paragraph 0005.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the type of processor to improve the functionality of the system.

Response to Arguments

8. Applicant's arguments filed on 8/30/2007 have been fully considered but are moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nov. 8, 2007

CHUN CAO
PRIMARY EXAMINER